REMARKS

Claims 1-7, 9-15, and 17-25 were pending in this application, and were each rejected.

Claim 24 has been amended to correct its dependency. The 35 USC § 112, paragraph 2 rejection is therefore believed to be obviated and is traversed.

Claims 1-7, 9-15, and 17-25 are now pending in this application.

Reconsideration and full allowance of Claims 1-7, 9-15, and 17-25 are respectfully requested.

I. REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 1-5, 8-13, 16-21 and 24 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,781,773 to Johnston *et al.* ("Johnston"). This rejection is respectfully traversed. Applicant respectfully notes that the Examiner also rejected claims 8 and 16 on this ground, although claims 8 and 16 were cancelled in the previous response.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. (*MPEP § 2131; In re Bond, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)*). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. (*MPEP § 2131; In re Donohue, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985)*).

Johnston describes an industrial controller permitting program editing during program execution, by placing new instructions in a second memory area, then placing conditional jump instructions to integrate the new instructions into the pre-existing program. Johnston does not

teach or suggest the limitations of independent Claims 1, 9, and 17. The Examiner does not actually indicate which elements he believes satisfy each of the claim limitations, instead referring to large passages of Johnson, so it is unclear where exactly the Examiner's misapprehension lies. If the Examiner maintains his rejection, Applicant respectfully requests that the Examiner identify by number those elements of Johnston on which he is relying, to clarify the arguments before appeal.

Claim 1 requires an apparatus for controlling a physical layer interface of a network interface card. Johnston does not so much as mention a network, or a network interface card, or a physical layer interface.

Claim 1 also requires a read only memory (ROM) capable of storing an embedded control program. Johnston teaches that memory unit 54 includes ROM (col. 5, lines 46-47) and that the processor 62 reads instructions of the relay ladder logic diagram from memory (col. 6, lines 1-3).

Claim 1 also requires a random access memory capable of storing a downloadable software control program downloaded from an external processing system. Johnston teaches that edited relay ladder instructions can be "entered by the user or by accessing a pre-stored file" (col. 8 lines 52-53. Nothing in this passage teaches storing a downloadable software control program downloaded from an external processing system. In particular, Johnston is silent as to where the "pre-stored filed" is stored or how it is entered.

Claim 1 also requires a microcontroller capable of controlling the physical layer interface, wherein said microcontroller in a first operating mode is capable of executing said embedded control program to thereby control said physical layer interface. Johnston does not

teach or suggest a microcontroller capable of controlling a physical layer interface of a network interface card, as claimed. Johnston does not teach or suggest that the relay ladder logic diagram is in any way capable of controlling a a physical layer interface of a network interface card, as claimed.

Claim 1 also requires that the microcontroller in a second operating mode is capable of executing said downloadable software control program in place of said embedded control program to thereby control said physical layer interface. Johnston does not teach or suggest this feature. Even assuming *arguendo* that the "new instructions" qualified as the claimed "downloadable software control program", these new instructions are never executed "in place of said embedded control program", as claimed. Instead, when the edit is complete, jump and branch instructions are added specifically to "integrate [the new instructions] into the pre-existing program" (col. 9, lines 20-21). That is, the pre-existing program executes without modification until the new instructions are integrated into the pre-existing program. There is no "first operating mode" where the pre-existing instructions are executed and a "second operating mode" where the new instructions are executed in place of the pre-existing instructions, as claimed.

Claim 1 also requires that the microcontroller comprises a plurality of control registers capable of controlling said first and second operating modes, wherein said microcontroller switches from said first operating mode to said second operating mode when said external processing system stores a jump address to said RAM in a first one of said plurality of control registers. This feature is not taught or suggested by Johnston. Johnston does not teach, suggest, discuss, or even mention registers at all.

Independent Claim 9 includes many limitations similar to those of claim 1, and so the arguments above apply to Claim 9 as well. In addition, Claim 9 requires a hard disk drive, which is not taught or suggested by Johnston at all. Claim 9 requires that the hard disk drive be capable of storing a network interface card (NIC) configuration file containing a downloadable software control program; Johnston does not teach or suggest anything like a network interface card (NIC) configuration file.

Independent Claim 17 requires in a first operating mode, executing an embedded control program stored in a read only memory (ROM) coupled to the microcontroller to thereby control the physical layer interface. This limitation is not taught or suggested by Johnston for reasons described above with relation to the claimed physical layer interface.

Claim 17 also requires, in a second operating mode, executing a software control program downloaded from an external processing system and stored in a random access memory (RAM) coupled to the microcontroller in place of the embedded control program to thereby control the physical layer interface. This limitation is not taught or suggested by Johnston for reasons described above with relation to the claimed first and second operating modes, and executing a downloaded program "in place of" the embedded program..

Claim 17 also requires switching from the first operating mode to the second operating mode when the external processing system stores a jump address to the RAM in a first one of a plurality of control registers in the microcontroller. This limitation is not taught or suggested by Johnston for reasons described above with relation to the claimed first and second operating modes, and with regard to the claimed registers.

For these reasons, Johnston fails to anticipate the Applicants' invention as recited in

Claims 1, 9, and 17 (and their dependent claims). Accordingly, the Applicants respectfully request withdrawal of the § 102 rejection and full allowance of Claims 1-5, 9-13, and 17-21.

II. REJECTION UNDER 35 U.S.C. § 103

Claims 6-7, 14-15, and 22-23 were rejected under 35 U.S.C. § 103(a) as being obvious over Johnston in view of U.S. Patent No. 6,859,825 to Williams ("Williams"). This rejection is respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the Applicant to produce evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the Applicant is entitled to grant of a patent. (*In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)*).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d*

781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on the Applicant's disclosure. (*MPEP § 2142*).

As shown above in Section I, Claims 1, 9, and 17 are patentable over Johnston. The claimed features described above as not taught or suggested by Johnston are similarly not taught or suggested by Williams. As a result, Claims 6, 7, 14, 15, 22, and 23 are patentable due to their dependence from allowable base claims.

Claim 25 was rejected as obvious over Johnston. The Examiner takes Official Notice that "one of ordinary skill in the art, [*sic*] would use 256 registers, each register filed [*sic*] containing 32 16-bit registers; [*sic*] because doing so would result in executing the updated control program that is taught by Johnston. This rejection is traversed.

Johnston does not teach the use of registers at all. The Examiner has provided no motivation at all to modify Johnston to use registers. The Examiner's statement "because doing so would result in executing the updated control program that is taught by Johnston" implies that Johnston does not operate as disclosed, if it requires non-disclosed registers in order to operate. This is not supported at all in Johnston. Of course, as Johnston does not teach or suggest the use

of registers at all, it certainly does not teach or suggest that the microcontroller includes 256 register files, each register file containing 32 16-bit registers, as in claim 25.

Finally, as the Examiner has taken Official Notice, he is cordially requested to support his official notice with documentary evidence by providing an affidavit or declaration setting forth specific factual statements and explanation to support the finding, as required by MPEP 2144.03. As the Examiner is surely aware, MPEP 2144.03 also clearly indicates that it would not be appropriate for the Examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known.

Accordingly, the Applicants respectfully request withdrawal of the § 103 rejection and full allowance of all claims.

All rejections have been traversed.

III. CONCLUSION

The Applicants respectfully assert that all pending claims in this application are in condition for allowance and respectfully request an early allowance of such claims.

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SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned attorney at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any fees connected with this communication (including any extension of time fees) or credit any overpayment to the Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

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Date: 02/27/06

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